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M.Tech. ECT

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY,

LONERE – RAIGAD – 402 103

Winter Semester Examination – December – 2018

Branch: M.Tech. (Electronics and Telecommunication Engineering) **Sem.: I**

Subject:- Microelectronics (MTEEC102/MTETE125E) **Marks: 60**

Date:- 12/12/2019 **Time: 3 Hrs.**

Instructions to the Students

1. Each question carries 12 marks.
2. Attempt any five questions of the following.
3. Illustrate your answers with neat sketches, diagram etc., wherever necessary.
4. If some part or parameter is noticed to be missing, you may appropriately assume it and should mention it clearly.

(Marks)

Q.1. a) Draw and explain the MOS diffusion capacitance model. **(06)**

b) Explain the operation of a tri state inverter. **(06)**

Q.2. a) Explain photolithography process in CMOS fabrication. **(06)**

b) Explain Gate and Source/Drain in formation in CMOS. **(06)**

Q.3. a) What is layout design? What are its approaches? Explain. **(06)**

b) Discuss CMOS process enhancements. **(06)**

Q.4. a) What is design margin? Explain. **(06)**

b) Explain RC delay model. **(06)**

Q.5. a) Explain CMOS multiplexers. **(06)**

b) Discuss static CMOS family. **(06)**

Q.6. a) Explain BiCMOS circuits. **(06)**

b) Explain CMOS inverter as an amplifier. **(06)**

Paper End