M.Tech. ECT

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD -402 103

END-SEM EXAMINATION Winter Examination – December 2019

Branch: M.Tech. (Electronics Engineering) **Sem.:- I**

Subject with Subject Code:- VLSI System Design (MTEEC103) **Marks: 60**

Date:- 17/12/2019 **Time:- 3 Hr.**

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Instructions:- i) Assume suitable data
ii) Attempt any five questions
iii) Each question carries twelve marks

Q.No.1 a)Draw dynamic latch circuit and explain it. Also draw stick diagram of a dynamic latch using transmission gate. (6)

b) What is function of re-circulating quasi static latch? Explain with diagram. (6)

Q.No.2 a) What is mean by Pseudo NMOS Logic? Why use a Pseudo-NMOS Logic? (6)

b) What is mean by Domino Logic? Illustrate a Domino OR Gate. (6)

Q.No.3 a) Design layout of CMOS Inverter and explain the layout design rule. (6)

b) Define Noise margin. Explain low noise and high noise margin with Transfer characteristics of CMOS Inverter. (6)

Q.No.4 a) Design the static Complementary pull up and pull down network for the following Function: (6)

i) F1= $\overline{(A+B+C)}$

ii) F2= $\overline{(A+B+C).D}$

b) How to reduce power consumption in CMOS logic ? Explain in detail (6)

Q.No.5 a) What is mean by Block Placement and Channel definition in Floor planning ? Elaborate in detail with diagram (6)

b) Draw a generic Integrated Circuit Design flow? Explain all steps in detail. (6)

Q.No.6 a) Define Logical effort. How to measure logical effort. Calculate the logical effort for Inverter, Two input NAND gate and two input NOR gate. (6)

b) What are the one phase clocking rules for Flip flops and two phase clocking disciplines for latches? (6)

Paper End