40T401405

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Mid Semester Examination – Oct 2018

Course: B. Tech in Electronics & Telecommunication Engineering **Sem: III**

Subject Name: Digital Logic Design **Subject Code: BTEXC305**

Max Marks: 20 **Date:- 12-10-18** **Duration:- 1 Hr.**

Instructions to the Students:

1. **Figure to right indicate full marks**
2. **Assume suitable data whenever necessary**

Marks

Q. 1 **6**

1. The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

A. AND
B. OR
C. NAND
D. None of Above

2. When grouping cells within a K-map, the cells must be combined in groups of _____.

A. 2's
B. 3's
C. 1,2,4,8…Etc.
D. 4's

3. How is a *J-K* flip-flop made to toggle?

A. J = 0, K = 0
B. J = 0, K = 1
C. J = 1, K = 0
D. J = 1, K = 1

4. Which of the following is correct for a Clocked *D* flip-flop?

A. The output toggles if one of the inputs is held HIGH.
B. Only one of the inputs can be HIGH at a time.
C. The output complement follows the input when enabled.
D. The output complement follows the input when enabled.

5. Which type of memory elements are used in synchronous sequential circuits?

a. Clocked Flip flops
b. Unclocked Flip flops
c. Time Delay Elements
d. All of the above

6. The major difference between a moore and mealy machine is that

A. output of the former depends on the present state and present input
B. output of the former depends only on the present state
C. output of former depends only on the present input
D. None of Above.

Q.2 Solve Any Two of the following. 3 X 2

(A) Solve K- Map for the equation

$F = \pi M (1,2,3,4,,6,7,8 ,) + d(4,5)$

(B) Convert JKFF to TFF

(C) Draw and explain four bit Universal Shift Register.

Q. 3 Solve Any One of the following. 8

(A) Design sequence generator using Mealy Machine for sequence 1 1 0

(B) Design 3- bit UP Counter.

*** End ***